REMARKS

Claims 1-33 are pending in the present application. Claims 1, 14, 26, 28, 30, and 32, and the specification have been amended to correct typographic errors, to respond to the rejections, and/or to further clarify the subject matter recited therein. No new matter is added by the amendments, which are supported throughout the specification and figures. In view of the amendments and the following remarks, favorable reconsideration of this case is respectfully requested.

Claims 1-33 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The Office Action asserts that the term the term "cache" as used in the specification and claims refers only to memory. However, the term "cache" can also be used to refer to a memory and an associated controller for reading and writing to the memory. Many of the sections of the specification used to describe the claimed cache make it apparent that references in the current disclosure to cache refer to a memory and controller combination. In particular, the each cache is described at one point as including a track location table 21 specific to the cache which gives its respective cache exact location details, on disks 12, for tracks of the range assigned to the cache (Specification; page 18, lines 17-22). Furthermore, the specification states that "[t]rack location table 21 may be implemented as software, hardware, or a combination of software and hardware" (Specification; page 18, lines 22-24). Furthermore, the specification indicates, with respect to figure 5, that:

> In a cache response 106, each cache 20 receiving a track request from the RRI responds to the request. The response is a function of, *inter alia*, the type of request, i.e., whether the track request is a read or a write command and whether the request is a "hit" or a "miss." Thus, data may be written to the LA of the track request from the cache and/or read from the LA to the cache. Data may also be written to the RRI from the cache and/or read from the RRI to the cache. If system 10 comprises an all-to-all configuration, and

> the response includes writing to or reading from the LA, the cache uses its track location table 21 to determine the location on the corresponding disk of the track for the LA.

(Specification; page 28, lines 12-25). As is apparent from the quoted passage, the caches discussed in the specification include associated controllers for the purpose of reading and writing the data to the respective cache. However, in the interest of expediting prosecution, Applicants herein amend the independent claims to clarify that each of the caches is implemented in separate physical units and adapted to function as controllers substantially independently of each other, as supported in the paragraph quoted above and throughout the specification and figures. Therefore, it is respectfully submitted that the claims as presented comply with the written description requirement.

Claims 1-13, 28, 29, 32, and 33 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Applicants respectfully traverse. Applicants respectfully disagree that the claims are directed to software, since a method is claimed. Applicants further disagree that software is non-statutory subject matter, since it is an article and a manufacture, as specified in 35 U.S.C. § 101. However, in the interest of expediting prosecution, Applicants herein amend the specification to clarify that the caches recited include dynamic RAM and/or solid state disks, and ***may also additionally comprise*** software. Therefore, the amended specification makes clear that the caches described therein include hardware. Therefore, it is respectfully submitted that the claims as presented are statutory.

Claims 1-8, 12-21, and 25 are rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent Publication No. 2004/0153727 to Hicken et al. (hereinafter referred to as Hicken). Applicants respectfully traverse.

Claim 1 relates to a method for managing a data storage system that includes, *inter alia*, configuring a first cache to perform at least one of the operations of retrieving data from and storing data at a first range of logical addresses (LAs) in a storage device, and configuring a second cache to perform at least one of the operations of retrieving data from and storing data at a first part of the first range of LAs. The method of amended claim 1 also includes configuring one or more third caches to perform at least one of the operations of retrieving data from and storing data at a second range of LAs in the storage device, ***the first, second and third caches being implemented in three separate physical units and adapted to function as controllers substantially independently of each other***. The method of claim 1 includes detecting an inability of the second cache to retrieve data from or store data at the first part of the first range of LAs. The method of amended claim 1 further includes ***reconfiguring at least one of the one or more third caches to perform at least one of the operations of retrieving data from and storing data at the first part of the first range of LAs in response to the inability while continuing to perform at least one of the operations of retrieving data from and storing data at the second range of LAs***.

The Examiner asserts that Hicken discloses a method for managing a data storage system (element 300 of Fig. 3; paragraph 0038, lines 4-10), as recited in claim 1. The Office Action apparently relies on element 339 as disclosure of a first cache, element 333 as disclosure of a second cache, and element 338 as disclosure of a third cache. However, as is apparent from figure 3 of Hicken, elements 338 and 339 do not operate ***substantially independently*** of each other. Rather, if CPU 336 fails, then both primary cache 338 and secondary cache 339 also fail. Therefore, the elements which the Office Action relies on as disclosing the caches of the present invention do not operate substantially independently.

Additionally, each of elements 333, 338 and 339 are not adapted to function as controllers, since they each have an associated CPU. More importantly, elements 338 and 339 are both controlled by the ***same*** CPU, and so they cannot be grouped with their respective CPU as operating substantially independently.

Furthermore, the Office Action asserts that element 338 discloses the one or more third cache as claimed. However, there is no disclosure relating to reconfiguring element 338 to perform the operations of retrieving data from and storing data at logical addresses which were previously serviced by element 333, which the Office Action asserts discloses the second cache. Nor is there any disclosure that element 338 in Hicken accepts these additional functions while continuing to perform at least one of the operations of retrieving data from and storing data at the second range of LAs, as claimed. Hicken merely discloses using a backup secondary cache memory for loading data in storage when a primary cache memory fails. Therefore, for at least all of the above reasons, claim 1 is allowable.

In stark contrast, in the present invention, ***the first, second, and third caches are implemented in three separate physical units and adapted to function as controllers substantially independently of each other***. In case of failure, Hicken transfers the responsibility previously defined for element 333 to element 339. In other words, unit 370-2 performs the functions previously performed by unit 370-1 and unit 370-2. In Hicken, element 339 is secondary to element 333, and when element 333 fails, 339 is then utilized fully. Hicken does not restore redundancy, but instead appears to bring the redundancy to bear by utilizing the redundant system as the primary system upon failure of the primary system, for instance, the failure of element 370-1. In the system according to Hicken, if element 370-2 fails after element 370-1 has failed, and before element 370-1 is repaired or replaced, ***then the entire system fails***.

In contrast, in the present invention, not only does the redundant system provide continuing performance in case of failure, but a second copy of the redundant copy is immediately produced and stored in a third, undamaged, cache. ***Redundancy is restored by immediately reconfiguring a third cache to perform the operations of retrieving data from and/or storing data at the first range of LAs***. Therefore, not only does the present invention allow the system to continue working, but the redundant state is also immediately restored so that if there is a second failure, the machine will still continue operating.

On page 31 of the present discussion, Applicants state that "[i]n system 140 each cache 20 is assumed to operate independently, so that failure or removal of one of the caches, or other action or fault causing the cache to become inoperative, has substantially no effect on the operation of the other caches" (Specification; page 30, lines 26-30). This is not the case in Hicken, in which caches are paired within one controller and when the controller fails, two caches become inoperative. As Hicken states:

> The first storage controller 130 includes a CPU 131, a program memory 132 (e.g. ROM/RAM devices for storing program instructions and variables for the operation of CPU 131), a primary cache memory 133 for storing data and control information related to the data stored in the disk array 140 and a secondary cache memory 134 for storing redundant data and control information related to the primary cache memory of another storage controller (for example the second storage controller 135). ***The CPU 131, the program memory 132, the primary cache memory 133 and the secondary cache memory 134 are connected via the memory bus 130-1 to enable the CPU 131 to store and retrieve information in the memory devices***. In addition, the first storage controller 130 includes tag memory 134-1, associated with or part of the secondary cache 134, that holds cache tags (the purpose and composition of the tag memory will be described below), also connected via the memory bus 130-1.

(Hicken; paragraph 0023; emphasis added). Additionally, paragraphs 0041-0043 of Hicken state that if controller 370-1 becomes inoperative, then two caches (333 which is primary and 334 which is secondary) simultaneously become inoperative. In Hicken, it is not possible to remove just one cache from the system, and the caches are always paired with a controller. In stark contrast, in the present invention, a cache is a self-contained entity that works alone and is not handled by a controller which also controls another cache. Hicken does not identically disclose or suggest that the first, second and third caches are implemented in three ***separate physical units*** and adapted to ***function as controllers substantially independently of each other***. Therefore claim 1 is allowable over the reference.

Independent claim 14 includes a feature similar to the feature discussed above in regard to claim 1, and therefore claim 14 is allowable for at least the same reasons as claim 1 is allowable.

Claims 2-8, 12, 13, 15-21, and 25 depend from one of claims 1 and 14, and therefore each of these claims is allowable for at least the same reasons as claims 1 and 14 are allowable.

Claims 26-33 are rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,898,666 to Henry et al. (hereinafter referred to as Henry). Applicants respectfully traverse.

Independent claims 26, 28, 30, and 32 have been amended to include a feature similar to the feature discussed above in regard to claim 1. Henry fails to disclose or suggest the feature of a plurality of interim fast-access-time caches, configured to operate ***as controllers substantially*** independently of one another, as recited in claim 26. Therefore, claim 26 is allowable over Henry.

Independent claims 28, 30, and 32 include features similar to the feature discussed above in regard to claim 26, and therefore each of these claims is allowable for at least the same reasons as claim 26 is allowable.

Claims 27, 29, 31, and 33 depend from one of claims 26, 28, 30, and 32, and therefore each of these claims is allowable for at least the same reasons as claims 26, 28, 30, and 32 are allowable.

Claims 9-11 and 22-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hicken in view of D. Karger et al. "Consistent Hashing and Random Trees: Distributed Caching Protocols for Relieving Hot Spots on the World Wide Web," Proceedings of the 29th ACM Symposium on Theory of Computing, pages 654-663, May 1997 (hereinafter referred to as Karger). Applicants respectfully traverse.

The addition of Karger fails to cure the critical deficiency discussed above in regard to Hicken as applied against claims 1 and 14. Therefore, since each of claims 9-11 and 22-24 depend from one of claims 1 and 14, each of these claims is allowable for at least the same reasons as claims 1 and 14 are allowable.

CONCLUSION

In view of the remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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